40Gbps 10km QSFP+ Transceiver
PQS40-3110

Features

- ✓ Supports 41.2Gbps aggregate bit rates
- ✓ Uncooled 4x10.3Gbps CWDM transmitter
- ✓ High-sensitivity PIN-TIA receiver
- ✓ Up to 10km on SMF
- ✓ Duplex LC receptacles
- ✓ Hot pluggable QSFP+ form factor
- ✓ Power dissipation < 3.5W
- ✓ All-metal housing for superior EMI performance
- ✓ RoHS6 compliant (lead free)
- ✓ Operating case temperature:
  Commercial: 0ºC to +70°C

Applications

- ✓ 40GBASE-LR4
- ✓ InfiniBand QDR and DDR interconnects
- ✓ 40G Telecom connections

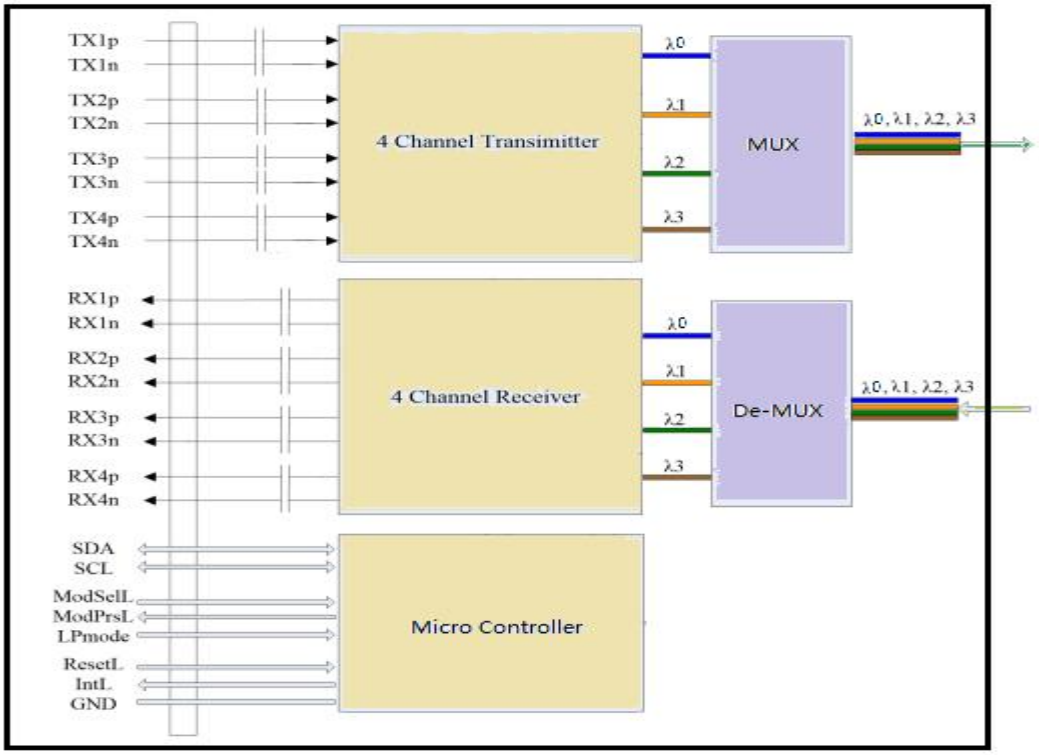
Standards

- ✓ Compliant with SFF-8436
- ✓ Compliant with SFF-8636
- ✓ Compatible with IEEE802.3ba

Description

The QSFP+ transceivers are designed for use in 40-Gigabit Ethernet links up to 10km over Single Mode Fiber. The transceivers are compatible with SFF-8436 and SFF-8636. For further information, please refer to SFF-8436 and SFF-8636.

Module Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Power Supply Voltage	V_{CC}	0		3.6	V
Storage Temperature	Ts	-40		+85	°C
Relative Humidity	RH	0		85	%
RX Input Average Power per Lane	P_{max}	-		3.5	dBm

Recommended Operating Environment

Parameter	Symbol	Min.	Typical	Max.	Unit
Power Supply Voltage	V_{CC}	3.13	3.3	3.46	V
Power Supply Current	I_{CC}			1000	mA
Power Dissipation	P_D			3.5	W
Operating Case Temperature	T_C	0		+70	°C
Aggregate Data Rate	-		41.25		Gbps
Bit Rate per Lane	BR		10.3125		Gbps

Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Transmitter Section						
Input Differential Impedance	R_{in}	90	100	110	Ω	
Differential Data Input Swing	$V_{in\ PP}$	180		1000	mV	1
Receiver Section						
Differential Data Output Swing	$V_{out\ PP}$	300		850	mV	

Notes:

1. Connected directly to TX data input pins. AC coupling from pins into laser driver IC.

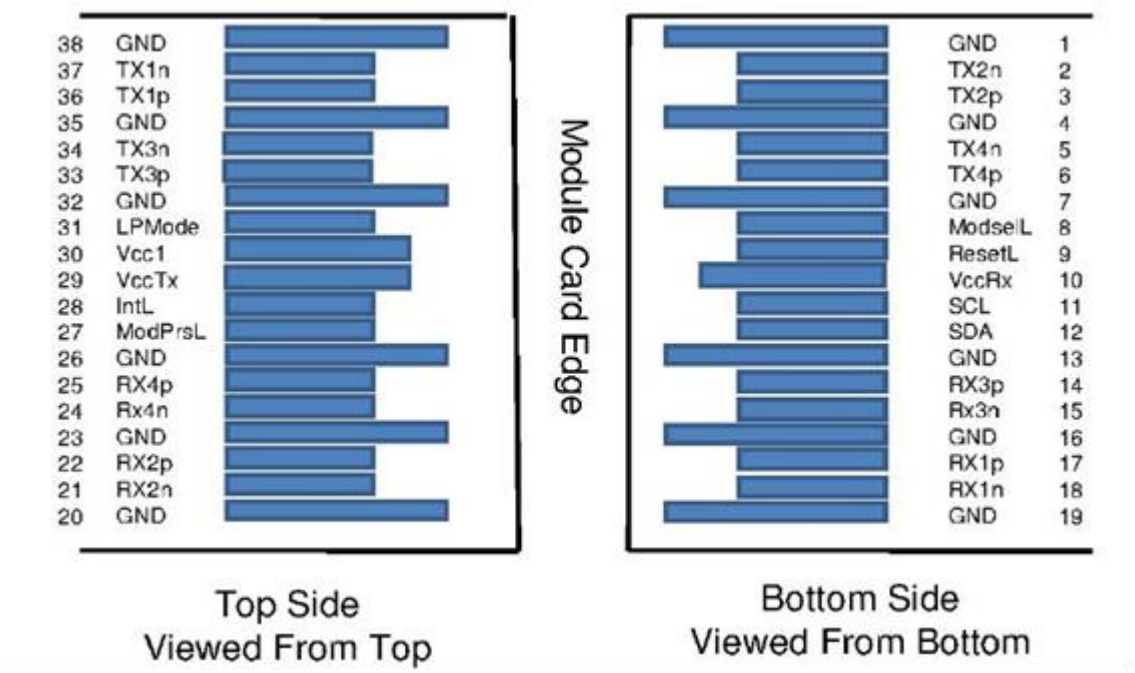
Optical Parameters

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Transmitter Section						
Lane Centre Wavelength (range)	λ_0	1264.5	1271	1277.5	nm	
	λ_1	1284.5	1291	1297.5	nm	
	λ_2	1304.5	1311	1317.5	nm	
	λ_3	1324.5	1331	1337.5	nm	
Spectral Width (-20dB)	Δλ			1	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Optical Power per Lane	P_{out}	-7.0		+2.3	dBm	1
OMA Power per Lane	OMA	-4		3.5	dBm	1
Laser Off Power per Lane	P_{off}	-	-	-30	dBm	
Extinction Ratio	ER	3.5	-	-	dB	2
Relative Intensity Noise	RIN	-	-	-128	dB/Hz	
Optical Return Loss Tolerance		-	-	20	dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	Compliant with IEEE802.3ba {0.25, 0.4, 0.45, 0.25, 0.28, 0.4}					2
Receiver Section						
Lane Center Wavelength (range)	λ_0	1264.5		1277.5	nm	
	λ_1	1284.5		1297.5	nm	
	λ_2	1304.5		1317.5	nm	
	λ_3	1324.5		1337.5	nm	
Average Receiver Power per Lane	RXP_X	-13.7		2.3	dBm	3
OMA Sensitivity per Lane	RX_{sens}			-11.5	dBm	3
Los Assert	LOS_A	-30	-	-	dBm	
Los Dessert	LOS_D	-	-	-16	dBm	
Los Hysteresis	LOS_H	0.5	-	5	dB	
Overload per Lane	$P_{in\text{-}max}$	-	-	2.3	dBm	3
Receiver Reflectance		-	-	-12	dB	
Damage Threshold per Lane		-	-	3.5	dBm	

Notes:

1. The optical power is launched into 9/125μm SMF.
2. Measured with a PRBS 2^{31}-1 test pattern @10.3125Gbps.
3. Measured with a PRBS 2^{31}-1 test pattern @10.3125Gbps, ER=4dB, BER <10^{-12}.

Pin Definitions



Pin Descriptions

Pin	Symbol	Description	Plug Seq.	Notes
1	Ground	Ground	1	1
2	Tx2n	Transmitter Inverted Data Input	3	
3	Tx2p	Transmitter Non-Inverted Data Input	3	
4	Ground	Ground	1	1
5	Tx4n	Transmitter Inverted Data Input	3	
6	Tx4p	Transmitter Non-Inverted Data Input	3	
7	Ground	Ground	1	1
8	ModSelL	Module Select	3	
9	ResetL	Module Reset	3	
10	VccRx	+3.3 V Power supply receiver	2	2
11	SCL	2-wire serial interface clock	3	
12	SDA	2-wire serial interface data	3	
13	Ground	Ground	1	1
14	Rx3p	Transmitter Non-Inverted Data Input	3	
15	Rx3n	Transmitter Inverted Data Input	3	

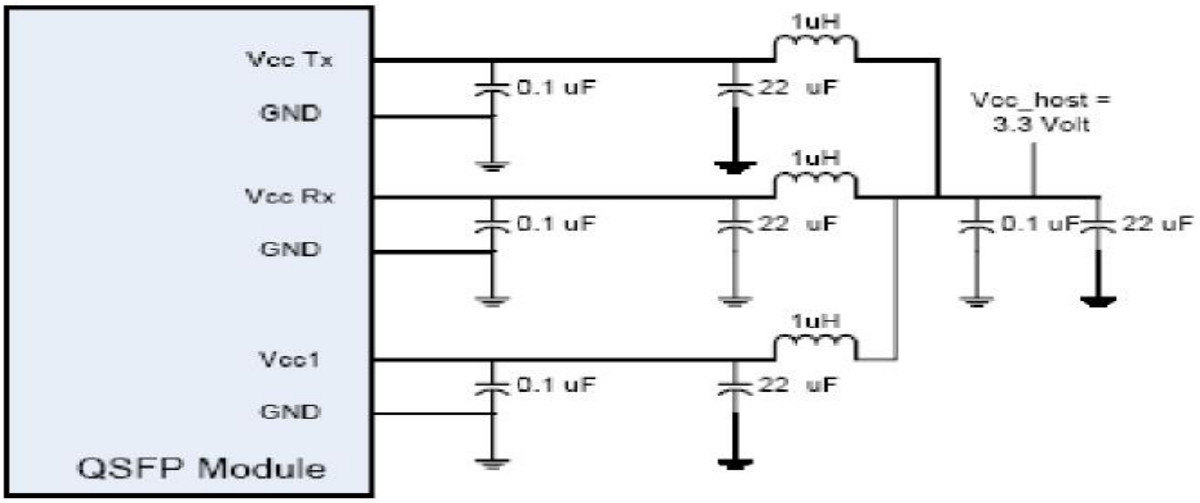
16	Ground	Ground	1	1
17	Rx1p	Transmitter Non-Inverted Data Input	3	
18	Rx1n	Transmitter Inverted Data Input	3	
19	Ground	Ground	1	1
20	Ground	Ground	1	1
21	Rx2n	Transmitter Inverted Data Input	3	
22	Rx2p	Transmitter Non-Inverted Data Input	3	
23	Ground	Ground	1	1
24	Rx4n	Transmitter Inverted Data Input	3	
25	Rx4p	Transmitter Non-Inverted Data Input	3	
26	Ground	Ground	1	1
27	ModPrsL	Module Present	3	
28	IntL	Interrupt	3	
29	VccTx	+3.3 V Power supply transmitter	2	2
30	Vcc1	+3.3 V Power Supply	2	2
31	LPMode	Low Power Mode	3	
32	Ground	Ground	1	1
33	Tx3p	Transmitter Non-Inverted Data Input	3	
34	Tx3n	Transmitter Inverted Data Input	3	
35	Ground	Ground	1	1
36	Tx1p	Transmitter Non-Inverted Data Input	3	
37	Tx1n	Transmitter Inverted Data Input	3	
38	Ground	Ground	1	1

Notes:

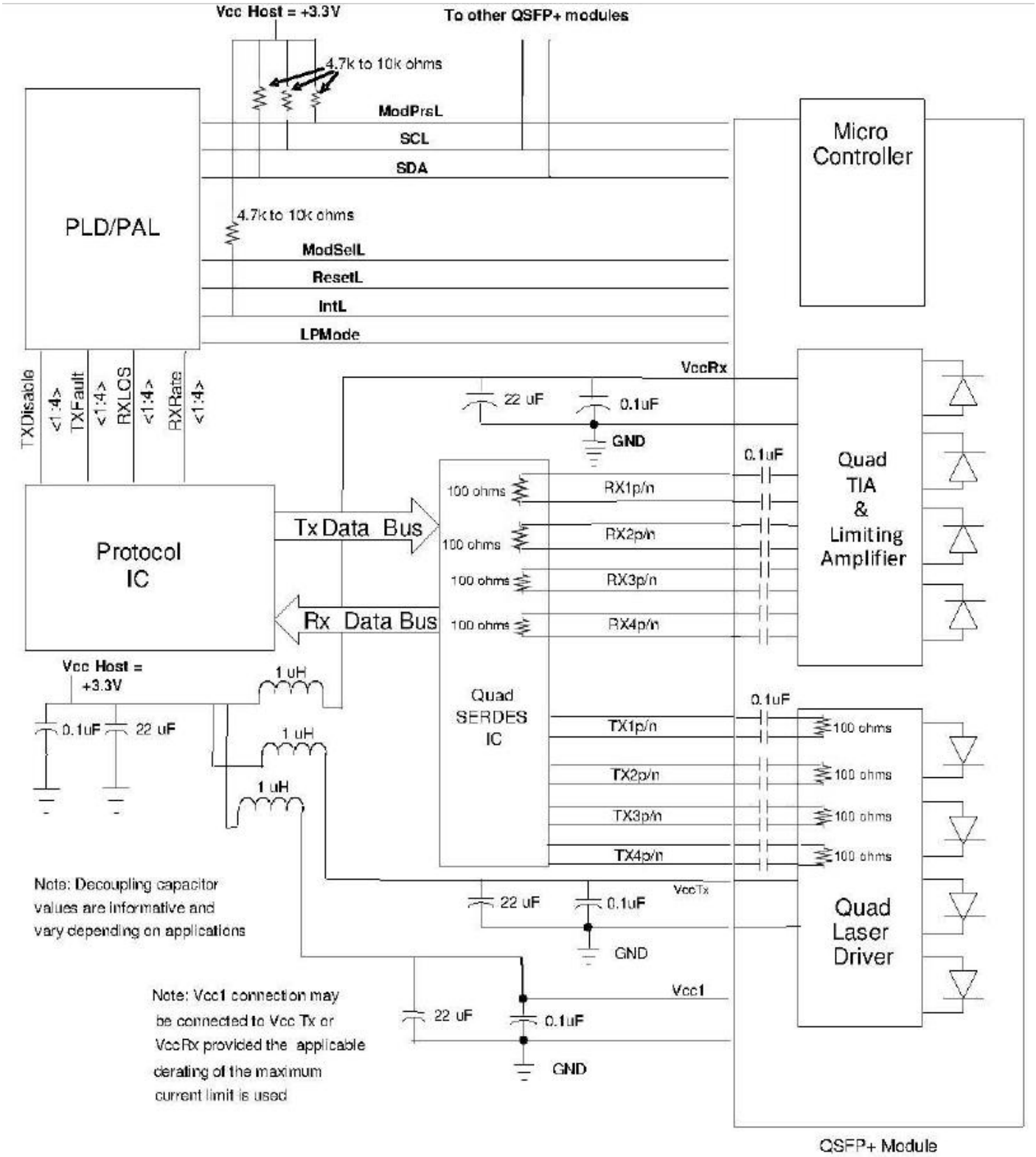
Plug Seq.: Pin engagement sequence during hot plugging.

1. Module ground pins GND are isolated from the module case.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power supplies and shall be applied concurrently.

Recommended Power Interface Circuit



Recommended Interface Circuit



Digital Diagnostic Functions

The QSFP+ transceivers support the 2-wire serial communication protocol as defined in the QSFP+ MSA, which allows real-time access to the following operating parameters:

- ✓ Transceiver temperature
- ✓ Laser bias current
- ✓ Transmitted optical power
- ✓ Received optical power
- ✓ Transceiver supply voltage

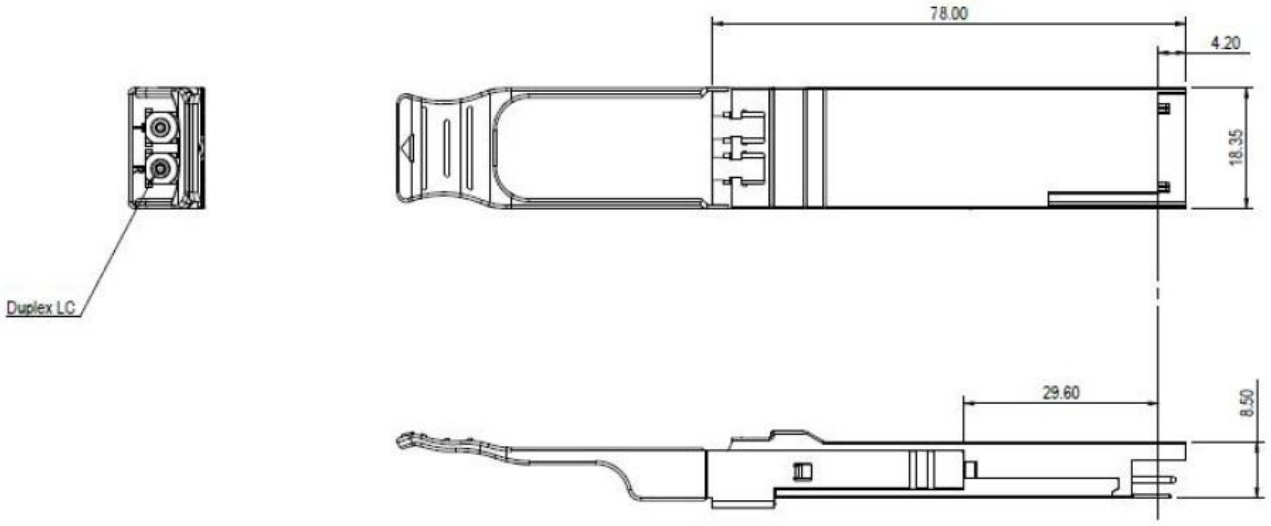
It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP+ transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP+ transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 00h to the maximum address of the memory.

This clause defines the Memory Map for QSFP+ transceiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP+ devices. The memory map has been changed in order to accommodate 4 optical channels and limit the required memory space. The structure of the memory is shown in Figure 2 QSFP+ Memory Map. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed. For example, in Figure 2 upper pages 01 and 02 are optional. Upper page 01 allows implementation of Application Select Table, and upper page 02 provides user read/write space. The lower page and upper pages 00 and 03 are always implemented. The interface address used is A0 and is mainly used for time critical data like interrupt handling in order to enable a “one-time-read” for all data related to an interrupt situation. After an Interrupt, IntL, has been asserted, the host can read out the flag field to determine the effected channel and type of flag.

For more detailed information including memory map definitions, please see the QSFP+ MSA Specification.

Mechanical Dimensions



Ordering information

Part Number	Product Description
PQS40-3110	40Gbps QSFP+ LR4, 10km on SMF, 0ºC ~ +70ºC, With DDM.

References

1. SFF-8436 Specification for QSFP+ Copper and Optical Transceiver, Rev 4.7, February 2013.
2. SFF-8636 Specification for Management Interface for Cabled Environments, Rev 2.6, June 2015.
3. IEE 802.3ba - PMD Type 40GBASE-LR4.

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